Application Hints
Fault-tolerant CAN transceiver

V2.0

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Changes compared to Version 1.0 :

1. Chapter 3, calculation examples for PCA82C252 and TJA1053 added, new aspects
2. Chapter 4, calculation hints for termination resistors added, new aspects

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1. Comparison PCA82C252 / TJA1053 / TJA1054

Reference for the below technical information is:

- Data sheet PCA82C252, revision Oct. 28, 1997
- Data sheet TJA1053, revision Oct. 15, 1997
- Data sheet TJA1054, revision Feb. 11, 1999

1.1. System parameters

Key	PCA82C252	TJA1053	TJA1054
System size	10 – 15 nodes [1) 2)]	10 – 15 nodes [2)]	> 32 nodes
Speed	20 - <125 kbps [3)]	20 – 125 kbps	40 – 125 kbps
Emission	+	+	++
Immunity	+	+	++
TxD dominant monitoring	no	yes	yes
Extended bus failure management (CANH to Vcc)	no	no	yes
Resolved problem of arbitration across open failures	no	yes	yes

1) The limit is given by the performance during CANH to ground failures, which very much depends on the size and type of cable used.
2) The limit is given by the wake-up capability during CANH to ground failures, which very much depends on the values of the distributed terminations across the network. Therefore, exact figures of system size cannot be given.
3) With CANH to VBAT failures the delay of the dominant edge is increased. The maximum speed strongly depends on the inductance of the cable used.

1.2. Device parameters

Key	PCA82C252	TJA1053	TJA1054
Current consumption in Normal Mode (I_{CC})	6 mA (recessive) 29 mA (dominant)	6 mA (recessive) 29 mA (dominant)	7 mA (recessive) 17 mA (dominant)
Current consumption in Standby Modes ($I_{BAT} + I_{CC}$)	70 uA	70 uA	30 uA
Minimum operating voltage	6V	6V	5V
Prevention of VBAT reverse current [1)]	no	no	yes
NWAKE sensitivity	negative edge	negative edge	both edges
Vcc Standby mode	yes	yes	no
NERR reporting of open failures	during frame only	during frame only	during frame and interframe space

1) In case a module looses its battery connection, a reverse power supply of this module via the CAN Bus lines is prevented. For the PCA82C252 and the TJA1053 an external diode at the battery pin of the Transceiver is required. This diode is required additionally to the control unit's polarity protection diode typically implemented at the battery connector of the entire module.

2. Series Resistor at Pin BAT of the TJA1053 / TJA1054

References for the below technical information are:

- Data sheet PCA82C252, revision Oct. 28, 1997
- Data sheet TJA1053, revision Oct. 15, 1997
- Data sheet TJA1054, revision Feb. 11, 1999

The following considerations are recommended for the determination of the series resistor (R_{BAT}) being attached to the supply input BAT (pin 14) of the TJA1053 / TJA1054 transceiver products.
The minimum recommended series resistance is about 1 kOhms for protection purpose against automotive transients. On the other hand the series resistance implies voltage drop on the battery supply and therefore lowers the minimum operating voltage. The voltage drop across the R_{BAT} series resistance can be calculated with the following consideration:

Sym.	Parameter	PCA82C252	TJA1053	TJA1054
V_{BAT}	Minimum operating voltage	6V	6V	5V
I_{BAT}	Basic BAT supply current (V_{BAT} = 12V)	75 uA	90 uA	50 uA (12V) 125 uA (5 to 27V)
I_{IL}	NWAKE input current	250 uA	70 uA	10 uA
I_{INH}	Max INH load (when used)	180 uA	180 uA	180 uA
R_{RTL}	RTL to V_{BAT} switch series resistance in low power modes	R_{RTL} = 10k to 28k	R_{RTL} = 8k to 23k	-
I_{RTL}	RTL current in low power modes	-	-	I_{RTL} = 0.3mA to 1.25mA
R_T	Bus termination resistance being attached to pin RTL	0.5k to 16k	0.5k to 16k	0.5k to 16k
I_{BATN}	Total BAT current in **normal mode**	75 uA + 250 uA + 180 uA = 505 uA	90 uA + 70 uA + 180 uA = 340 uA	125 uA + 10 uA + 180 uA = 315 uA
	Max R_{BAT} voltage drop with R_{BAT} = 1k in normal mode	0.51V	0.34V	0.32V
I_{RTL}	Max RTL load (applies only to low-power modes)	$V_{BAT}/(R_{RTL} + R_T)$ = 12V/(8k + 0.5k) = 1.41 mA	$V_{BAT}/(R_{RTL} + R_T)$ = 12V/(8k + 0.5k) = 1.41 mA	1.25 mA
I_{BATL}	Total BAT current in **low-power mode** (V_{BAT} = 12V)	0.51 mA + 1.41 mA = 1.92 mA	0.34 mA + 1.41 mA = 1.75 mA	0.32 mA + 1.25 mA = 1.57 mA
	Max R_{BAT} voltage drop with R_{BAT} = 1k in low-power mode (V_{BAT} = 12V)	1.92V	1.75V	1.57V

The recommended range for the series resistor being attached to the supply pin BAT is 1 kΩ to 2 kΩ.

3. Vcc Supply and Recommended Bypass Capacitance

References for the below technical information are:

- Data sheet PCA82C252, revision Oct. 28, 1997
- Data sheet TJA1053, revision Oct. 15, 1997
- Data sheet TJA1054, revision Feb. 11, 1999

3.1. List of used Abbreviations

Table 3-1 : Used abbreviations

Symbol	Description
I_{cc_dom}	Supply current at pin VCC while driving a dominant bit **with** a certain load to the pins
I_{cc0_dom}	Supply current at pin VCC while driving a dominant bit **without** any load to the pins
I_{CANH_dom}	Output current of pin CANH while driving a dominant bit with nominal bus load of 100 Ohms in total
I_{RTL_dom}	Output current of pin RTL while driving a dominant bit with a certain load
I_{cc_rec}	Supply current at pin VCC while driving a recessive bit
$I_{cc\_norm\_avg}$	Average supply current at pin VCC assuming no bus failure and continuous sending
$I_{cc\_sc1\_dom}$	Supply current at pin VCC driving a dominant bit while CANH is shorted to GND
$I_{CANH\_sc1\_dom}$	Output current of pin CANH driving a dominant bit while CANH is shorted to GND
$I_{cc\_sc1\_avg}$	Average supply current at pin VCC assuming CANH shorted to GND and continuous sending
ΔI_{cc_sc1}	Supply current change at pin VCC in case a dominant bit is driven while CANH is shorted to GND
$I_{cc\_sc2\_dom}$	Supply current at pin VCC driving a dominant bit while CANH **and** CANL are shorted to GND
$I_{RTL\_sc\_dom}$	Output current of pin RTL while driving a dominant bit with CANL shorted to GND
ΔI_{cc_sc2}	Supply current change at pin VCC in case a dominant bit is driven while CANH and CANL are shorted to GND
V_{CC}	Supply voltage at pin VCC
V_{CANL_dom}	Voltage level on CANL while a dominant bit is driven
R_T	Termination resistor connected to pins RTL and RTH
t_{dom_max}	Maximum possible continuous dominant drive time
ΔV_{max}	Maximum allowed voltage change at pin VCC
C_{BUFF}	Required buffer capacitance in case the voltage regulator does not deliver extra current within t_{dom_max}

3.2. Summary

In order to properly dimension the Vcc supply of the Fault-Tolerant CAN Transceivers two parameters have to be taken into account:

1) the average supply current
2) the peak supply current

The average supply current is needed to calculate the thermal load of the required Vcc voltage regulator. The peak supply current may flow in case of certain bus failure conditions for a certain time and thus has an impact on the power supply buffering.

The Vcc supply of the Transceiver is recommended to support the characteristics as follows:

Table 3-2 : Overview of supply currents

Item	PCA82C252	TJA1053	TJA1054
Average Vcc supply current without bus failures	44.5 mA	44.5 mA	41 mA
Average Vcc supply current at presence of single bus failures	74.5 mA	74.5 mA	76 mA
Worst case peak Vcc supply current at presence of single bus failure (for 6 bit times max.)	139 mA	139 mA	141 mA
Worst case peak Vcc supply current at presence of dual bus failures (for 17 bit times max.)	140 mA	140 mA	142 mA

The capacitive buffering needed for the transceiver depends on the systems power concept and the regulator characteristic of the used voltage regulator chip.

In case the transceiver has a **separated** Vcc power supply independently from the microcontroller, the peak supply current during single bus failures is relevant because here the communication medium has to keep unaffected. The worst case dual failure situation is not relevant since here the communication medium is completely unavailable and the transceiver does not needed to be supplied anymore. Such systems are recommended to provide a bypass capacitance of **47 uF** in order to withstand single wiring faults. **Depending on the regulator behaviour this capacitance may become smaller if the regulation time constant is fast enough.**

In case the transceiver's Vcc power supply is **shared** with its host microcontroller, the peak supply current during the worst case dual failure situation has to be taken into account. This is because the uC has to keep a proper supply even if there is no CAN communication possible at all. Such systems are recommended to provide a bypass capacitance of **150uF**. **Depending on the regulator behaviour this capacitance may become much smaller if the regulation time constant is fast enough.**

This capacitance can be implemented as a separate component or alternatively through a corresponding increase of the capacitance of the bypass capacitor being located at the Vcc voltage regulator.

In the following, relevant cases are considered in more detail.

3.3. Average Supply Current at Absence of Bus Short-Circuit Conditions

In recessive state the Transceivers are consuming a Vcc supply current as listed in the corresponding data sheets. In dominant state the Vcc supply current is calculated by the addition of the IC-internal supply current (Data sheet, no load condition) and the output current at pins CANH and RTL.

3.3.1. Maximum dominant supply current (without bus wiring faults)

$$I_{cc\_dom} = I_{cc0\_dom} + I_{CANH\_dom} + I_{RTL\_dom} \quad (1)$$

$$I_{RTL\_dom} = (Vcc - V_{CANL\_dom}) / R_T \quad (2)$$

3.3.2. Example calculation

Maximum dominant supply current without bus wiring faults:

Item from Data Sheet / Assumptions	*Symbol*	*PCA82C252*	*TJA1053*	*TJA1054*
Max. Vcc supply current dominant, no load	I_{cc0_dom}	35 mA	35 mA	27 mA
CANH dominant current	I_{CANH_dom}	40 mA	40 mA	40 mA
Assumed termination resistor	R_T	1 k	1 k	1 k
Assumed CANL dominant voltage	V_{CANL_dom}	1 V	1 V	1 V

PCA82C252 : $I_{cc\_dom\ 252}$ = 35mA + 40 mA + (5V - 1V) / 1k = 79 mA max. (Ex 1.1)

TJA1053 : $I_{cc\_dom\ 1053}$ = 35mA + 40 mA + (5V - 1V) / 1k = 79 mA max. (Ex 1.2)

TJA1054 : $I_{cc\_dom\ 1054}$ = 27mA + 40 mA + (5V - 1V) / 1k = 71 mA max. (Ex 1.3)

3.3.3. Thermal considerations (without bus wiring faults)

For thermal considerations the average supply current at pin Vcc is relevant considering the transmit duty cycle. In the following example a continuously transmitting node is assumed. This might happen e.g. if a node starts a transmission while the rest of the network does not respond with an acknowledge for some reason. Typically a much lower duty cycle is relevant since a node transmits messages within certain time slots only, depending on the applications network management.

With an assumed transmit duty cycle of 50% on pin TxD, the maximum average supply current is

$$I_{cc\_norm\_avg} = 0.5 * (I_{cc\_rec} + I_{cc\_dom}) \quad (3)$$

3.3.4. Example calculation

Thermal considerations without bus wiring faults:

Item	*Symbol*	*PCA82C252*	*TJA1053*	*TJA1054*
Vcc supply current recessive, max.	I_{cc_rec}	10 mA	10 mA	11 mA

PCA82C252 : $I_{cc\_norm\_avg\ 252}$ = 0.5 * (10mA + 79mA) = **44.5 mA max.** (Ex 3.1)

TJA1053 : $I_{cc\_norm\_avg\ 1053}$ = 0.5 * (10mA + 79mA) = **44.5 mA max.** (Ex 3.2)

TJA1054 : $I_{cc\_norm\_avg\ 1054}$ = 0.5 * (11mA + 71mA) = **41 mA max**. (Ex 3.3)

3.4. Average Supply Current at Presence of a Short-Circuit of one Bus Wire

The maximum Vcc supply current occurs with a bus wire short-circuit between CANH and GND. In this case the CANH outputs a maximum short circuit current in dominant state (see data sheets). For thermal considerations the average supply current is relevant. For buffering considerations the maximum dominant supply current is relevant.

3.4.1. Maximum dominant supply current (with CANH shorted to GND)

$$I_{cc\_sc1\_dom} = I_{cc0\_dom} + I_{CANH\_sc1\_dom} + I_{RTL\_dom} \quad (t \leq 6 \text{ bit times}) \qquad (4)$$

The 6-bit time limitation is caused by a supposed Error Flag to be sent by the CAN Controller.

3.4.2. Example calculation

Maximum dominant supply current with CANH shorted to GND:

Item	*Symbol*	*PCA82C252*	*TJA1053*	*TJA1054*
CANH dominant current, short circuit	$I_{CANH\_sc1\_dom}$	100 mA	100 mA	110 mA

PCA82C252 : $I_{cc\_sc1\_dom\ 252}$ = 35mA + 100 mA + (5V - 1V) / 1k = **139 mA max.** (Ex 4.1)

TJA1053 : $I_{cc\_sc1\_dom\ 1053}$ = 35mA + 100 mA + (5V - 1V) / 1k = **139 mA max.** (Ex 4.2)

TJA1054 : $I_{cc\_sc1\_dom\ 1054}$ = 27mA + 110 mA + (5V - 1V) / 1k = **141 mA max.** (Ex 4.3)

3.4.3. Thermal considerations (with CANH shorted to GND)

For thermal considerations the average supply current at pin Vcc is relevant considering the transmit duty cycle. With a transmit duty cycle of 50% on pin TxD, the maximum average supply current at CANH to GND short-circuit is:

$$I_{cc\_sc1\_avg} = 0.5 * (I_{cc\_rec} + I_{cc\_sc1\_dom}) \qquad (5)$$

3.4.4. Example calculation

Thermal considerations with CANH shorted to GND:

PCA82C252 : $I_{cc\_sc1\_avg\ 252}$ = 0.5 * (10mA + 139mA) = **74.5 mA max.** (Ex 5.1)

TJA1053 : $I_{cc\_sc1\_avg\ 1053}$ = 0.5 * (10mA + 139mA) = **74.5 mA max.** (Ex 5.2)

TJA1054 : $I_{cc\_sc1\_avg\ 1054}$ = 0.5 * (11mA + 141mA) = **76 mA max.** (Ex 5.3)

3.4.5. Vcc extra supply current in single fault condition

Compared to the quiescent current in recessive state the maximum **extra** supply current when the CANH driver is turned on with CANH shorted to GND is needed to calculate the required worst case Vcc buffer capacitance. This extra supply current has to be buffered for up to 6 bit times, depending on the applications voltage regulator.

$$\Delta I_{cc\_sc1} = I_{cc\_sc1\_dom} - I_{cc\_rec} \quad \textbf{(6)}$$

3.4.6. Example calculation

Vcc extra supply current in case of dual fault condition.

Item	*Symbol*	*PCA82C252*	*TJA1053*	*TJA1054*
Min Vcc supply current, recessive	I_{cc_rec}	3,5 mA [1)]	3,5 mA [1)]	4 mA

1) The minimum quiescent current is estimated since this value is not specified for the PCA82C252 and the TJA1053.

PCA82C252 : $\Delta I_{cc\_sc1\ 252}$ = 139 mA - 3.5 mA = **135.5 mA max.** (Ex 6.1)

TJA1053 : $\Delta I_{cc\_sc1\ 1053}$ = 139 mA - 3.5 mA = **135.5 mA max.** (Ex 6.2)

TJA1054 : $\Delta I_{cc\_sc1\ 1054}$ = 141 mA - 4 mA = **137 mA max.** (Ex 6.3)

3.5. Worst Case Max Vcc Supply at Presence of a Dual Short Circuit

The worst case max. Vcc supply current is flowing in case of a **dual short-circuit** of the bus lines CAN_H and CAN_L to ground. In this case no communication is possible. Nevertheless the application supply should be able to deliver a proper Vcc for the microcontroller in order to prevent erroneous operation.
If there is a **separate** voltage regulator available supplying the transceiver exclusively, **no care** has to be taken on this dual short circuit condition since the transceivers are behaving fail safe in case of under voltage conditions and the uC is still powered properly by its own supply.

In case of a **shared** voltage supply of transceiver and microcontroller this dual fault condition is relevant to dimension the required buffer capacitor.

3.5.1. Max Vcc supply current in worst case dual fault condition

$$\mathbf{I_{cc\_sc2\_dom} = I_{cc0\_dom} + I_{CANH\_sc1\_dom} + I_{RTL\_sc\_dom}} \qquad \mathbf{(t \leq 17 \text{ bit times })} \qquad \mathbf{(7)}$$

$$\mathbf{I_{RTL\_sc\_dom} = Vcc / R_T} \qquad \mathbf{(8)}$$

The 17-bit time limitation is caused by the CAN protocol. Due to the dual fault condition with CANH and CANL shorted to GND the RxD pin of the transceiver is continuously clamped recessive (CANL to GND forces CANH operation; CANH is clamped recessive).

The moment the CAN controller starts a transmission, this dominant Start Of Frame bit is not fed back via RxD and thus forces an error flag due to the bit failure condition (TX Error Counter increment by 8). This first bit of the error flag again is not reflected at RxD and forces the next error flag (TX Error Counter + 8).

Latest after 17 bit times, depending on the TX Error Counter Level before starting this transmission, the CAN controller reaches the Error Passive limit (128) and stops sending dominant bits. Now a sequence of 25 recessive bits follows (8 Bit Error Delimiter + 3 Bit Intermission + 8 Bit Suspend Transmission) and the Vcc current becomes reduced to the recessive one.
From now on only single dominant bits (Start Of Frame) followed by 25 recessive bits (Passive Error Flag + Intermission + Suspend Transmission) are output until the CAN controller enters the Bus Off State.

So, for dimensioning the Vcc voltage source in this worst case dual failure scenario, up to 17 bit times might have to be buffered by a bypass capacitor depending on the regulation capabilities of the used voltage supply.

3.5.2. Example calculation

Max Vcc supply current in worst case dual fault condition:

PCA82C252 :	$I_{cc\_sc2\_dom\ 252}$ = 35 mA + 100 mA + 5V / 1k = **140 mA max.**	(Ex 7.1)
TJA1053 :	$I_{cc\_sc2\_dom\ 1053}$ = 35 mA + 100 mA + 5V / 1k = **140 mA max.**	(Ex 7.2)
TJA1054 :	$I_{cc\_sc2\_dom\ 1054}$ = 27 mA + 110 mA + 5V / 1k = **142 mA max.**	(Ex 7.3)

3.5.3. Vcc extra supply current in dual fault condition

Compared to the quiescent current in recessive state the maximum **extra** supply current when the CANH driver is turned on in dual short-circuit condition is needed to calculate the required worst case Vcc buffer capacitance. This extra supply current has to be buffered for that time the applications voltage regulator needs to react.

$$\Delta I_{cc\_sc2} = I_{cc\_sc2\_dom} - I_{cc\_rec} \quad \textbf{(9)}$$

3.5.4. Example calculation

Vcc extra supply current in case of dual fault condition.

Item	*Symbol*	*PCA82C252*	*TJA1053*	*TJA1054*
Min Vcc supply current, recessive	I_{cc_rec}	3,5 mA [1)]	3,5 mA [1)]	4 mA

1) The minimum quiescent current is estimated since this value is not specified for the PCA82C252 and the TJA1053.

PCA82C252 : $\Delta I_{cc\_sc2\ 252}$ = 140 mA - 3.5 mA = **136.5 mA max.** (Ex 9.1)

TJA1053 : $\Delta I_{cc\_sc2\ 1053}$ = 140 mA - 3.5 mA = **136.5 mA max.** (Ex 9.2)

TJA1054 : $\Delta I_{cc\_sc2\ 1054}$ = 142 mA - 4 mA = **138 mA max.** (Ex 9.3)

3.6. Calculation of worst-case bypass capacitor

Depending on the power supply concept, the required worst-case bypass capacitor can be calculated. In case of a **separate Vcc** supply for the transceiver only, the extra supply current ΔI_{cc_sc} in case of the **single fault condition** has to be taken with a maximum of 6 dominant bit times.

If the transceiver and the host microcontroller are supplied from the same regulator (**shared Vcc supply**), the extra supply current ΔI_{cc_sc} in case of the **dual fault condition** has to be taken with a maximum of 17 dominant bit times.

$$C_{BUFF} = \Delta I_{cc\_sc} * t_{dom\_max} / \Delta V_{max} \quad \textbf{(10)}$$

The capacitor C_{BUFF} is needed if the voltage regulator is **not** able to deliver any extra current within the maximum dominant output drive t_{dom_max} during the dual fault condition.

3.6.1. Example calculation, separate supplied transceiver @ 83,33kBit/s

In case of a separate transceiver supply the bypass capacitance has to be calculated based on the single fault condition with CANH shorted to GND. Here the dual fault is not relevant.

Assumption of 83,33 kBit/s : t_{dom_max} = 6 * 12 us = 72 us
Maximum allowed Vcc voltage drop : ΔV_{max} = 0.25V

PCA82C252 : $C_{BUFF\ 252}$ = 135.5 mA * 72 us / 0.25 V = **39 uF** (Ex 10.1)

TJA1053 : $C_{BUFF\ 1053}$ = 135.5 mA * 72 us / 0.25 V = **39 uF** (Ex 10.2)

TJA1054 : $C_{BUFF\ 1054}$ = 137 mA * 72 us / 0.25 V = **39,5 uF** (Ex 10.3)

In this example the bypass capacitance to be reserved for the Vcc supply of the Transceiver is recommended to be 39,5 uF minimum at 83,33 kBit/s. It may become smaller, if the used voltage regulator is able to deliver an extra current within t_{dom_max}.

3.6.2. Example calculation, shared supply

In case of a shared supply concept the bypass capacitance has to be calculated based on the worst case dual fault condition in order to keep the uC supply stabile:

Assumption of 83,33 kBit/s : t_{dom_max} = 17 * 12 us = 204 us
Maximum allowed Vcc voltage drop : ΔV_{max} = 0.25V

PCA82C252 : $C_{BUFF\ 252}$ = 136.5 mA * 204 us / 0.25 V = **111.4 uF** (Ex 10.1)

TJA1053 : $C_{BUFF\ 1053}$ = 136.5 mA * 204 us / 0.25 V = **111.4 uF** (Ex 10.2)

TJA1054 : $C_{BUFF\ 1054}$ = 138 mA * 204 us / 0.25 V = **113 uF** (Ex 10.3)

In this example the bypass capacitance to be reserved for the Vcc supply of the Transceiver is recommended to be 113 uF minimum at 83,33 kBit/s. It may become smaller, if the used voltage regulator is able to deliver an extra current within t_{dom_max}.

4. Calculation of Bus Termination Resistors and EMC issues

4.1. How to dimension the Bus Termination Resistor values, some basic rules

The fault tolerant transceivers are designed to deliver optimum system behaviour at a total termination resistance of 100 Ohms. This means that the CANH line is terminated with 100 Ohms as well as the CANL line. Because the termination of this fault tolerant system is distributed all over the network, each of the transceivers has to deliver only a part of the total 100 Ohm termination. So depending on the overall system size the single nodes local termination resistors have to be calculated.

Termination resistors are connected within each control unit to the corresponding RTH and RTL pins of the transceivers.

Examples :

5 node system : 500 Ohms termination at each transceiver,

10 node system : 1000 Ohms termination at each transceiver

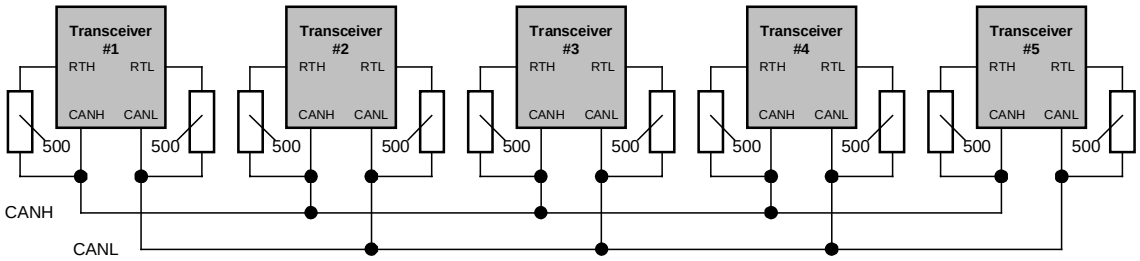


Fig. 1 : Example Network with 5 nodes, 500 Ohms termination at each node

It is not required that each transceiver in the system has the same termination resistor value. In total the termination should result in 100 Ohms. It is not recommended to terminate the entire system lower than 100 Ohms since the CAN output drivers are limited to a load of 100 Ohms.

The minimum termination resistor value allowed per transceiver is 500 Ohms due to the driving capability of the RTL and RTH pins. So within systems with less than 5 transceivers it is not possible to achieve the 100 Ohm termination optimum. In practice this is typically no problem because such “small” systems will have less bus cable lengths compared to bigger networks and thus have no problem with a higher total termination resistances.

It is recommended not to exceed approximately 6kOhms termination at a single transceiver in order to provide a good EMI (Electro Magnetic Immunity) performance of the system in case of interrupted bus wires. Nevertheless up to 16kOhms are specified for the transceivers.

4.1.1. Variable System Size, Optional Nodes

In case of variable system sizes with optional nodes it is recommended to achieve a total termination resistance close to 100 Ohms provided by the standard nodes which are always present. The optional nodes should have the higher termination resistances then. Due to EMI issues it is recommended not to exceed approx. 6kOhms for the optional nodes.

4.1.2. Example calculation, Variable System Size

The entire example system has 15 nodes in total, 5 nodes of this system are optional ones and only implemented if required:

Termination of the 10 standard nodes :	1.2 kOhm per node
Termination of the 5 optional nodes :	3 kOhm per node
Total system termination, standard nodes only :	1.2 kOhm / 10 nodes =
	120 Ohms (...close to 100)
Total system termination, 15 nodes :	(3 kOhm / 5 nodes) parallel to 120 Ohms =
	100 Ohms

There is no general rule how to distribute the termination within the network. A rule of thumb is :

“The longer the cable stub, the lower the local termination.”

4.2. Tolerances of Bus Termination Resistors, EMC Considerations

The symmetry of the termination resistors within a single node has a major impact to the systems EME (Electro Magnetic Emission) behaviour. Thus it is important to have well matched termination resistors within each control unit. This means that the RTH resistor should have exactly the same value compared to the RTL resistor within one control unit in order to get the same time constant on each bus wire during signal transitions. The tolerance between two different control units is absolutely insignificant (see also 4.1.1.).
The principle to achieve a good EME performance is that the differential signal on the bus wires eliminates any emission due to compensation effects if both CAN wires are carrying exactly the same signal, but with inverse polarities.
Here the transceiver can only provide a perfect symmetry for the dominant transitions by design. The recessive transitions are mainly driven by the termination resistors and the network cables itself. So not only the transceiver’s output drivers have an impact to the EME performance but also the termination and the cable symmetry.

It is recommended to provide a termination resistor accuracy (RTH compared to RTL) within the same node of 1% or lower. Also the bus cable has to be at least a twisted pair cable in order to achieve a symmetrical capacitive load for both bus wires resulting in a good EMC performance.

It is obvious that also the layout of printed circuit boards has a significant impact to the EMC behaviour if the CAN lines have different capacitive loads due to different wire lengths.

4.3. Output Current and Power Dissipation of Bus Termination Resistors R_T

References for the below technical information are:

- Data sheet PCA82C252, revision Oct. 28, 1997
- Data sheet TJA1053, revision Oct. 15, 1997
- Data sheet TJA1054, revision Feb. 11, 1999

4.3.1. Summary

The bus termination resistors R_T being connected to the fault tolerant transceivers are recommended to withstand the following power dissipations (@ $R_T \geq 1000$ Ohms):

PCA82C252 : 64 mW
TJA1053 : 64 mW
TJA1054 : 23,7 mW

The following chapters are discussing this issue in more detail.

4.3.2. Average power dissipation, no bus failures

In order to dimension the power dissipation of the termination resistors the average power dissipation between dominant and recessive bits has to be taken into account. Additionally a worst case ground offset of the certain module has an impact.
CAN frames are assumed to have a ratio of dominant bits in the range of 0.75 worst case because of stuffing and fixed recessive frame segments. Thus the average power dissipation is calculated as follows:

$$\mathbf{P_{avg} = (0.75 * (V_{cc} + V_{GND}))^2 / R_T} \quad \mathbf{(11)}$$

4.3.3. Example calculation, average power dissipation

Assumption : $R_T = 1000$ Ohms

$P_{avg} = (0.75 * (5V + 1{,}5V))^2 / 1000\ \text{Ohms} = \mathbf{23.7\ mW}$ (Ex 11.1)

4.3.4. Maximum continuous power dissipation

Because the PCA82C252 and the TJA1053 do not provide a failure detector for CANH short circuits to Vcc the maximum continuous current flows in case CANH has a short circuit to 8V. This is the maximum detection threshold for CANH to Battery short circuit conditions.

For the TJA1054 this threshold is 1.85V since shorts to Vcc are detected by this transceiver.

$$\mathbf{P_{cont} = (V_{det\ max})^2 / R_T} \quad \mathbf{(12)}$$

4.3.5. Example calculation, maximum continuous power dissipation

Assumption : $R_T = 1000$ Ohms

PCA82C252 : $P_{cont} = (8\ V)^2 / 1000\ \text{Ohms} = \mathbf{64\ mW}$ (Ex 12.1)
TJA1053 : $P_{cont} = (8\ V)^2 / 1000\ \text{Ohms} = \mathbf{64\ mW}$ (Ex 12.2)
TJA1054 : $P_{cont} = (1.85\ V)^2 / 1000\ \text{Ohms} = \mathbf{3.4\ mW}$ (Ex 12.3)

4.3.6. Maximum peak power dissipation

A peak current will flow in case of short circuits of CANH to VBAT. After the device specific detection time, the bus failure detector will switch off the bias on RTH. Thus this peak current does only flow for a short time.

$$P_{peak} = V_{BAT}^2 / R_T \qquad (t < t_{det\_HBAT}) \qquad (13)$$

4.3.7. Example calculation, maximum peak power dissipation

Item	*Symbol*	*PCA82C252*	*TJA1053*	*TJA1054*
Maximum Failure Detection Time, CANH shorted to VBAT	t_{det_HBAT}	60 us	60 us	8 ms

Assumptions : R_T = 1000 Ohms, V_{BAT} = 27V

PCA82C252 : P_{peak} = (27 V) ^{2} / 1000 Ohms = **730 mW** for less than **60 us** (Ex 13.1)

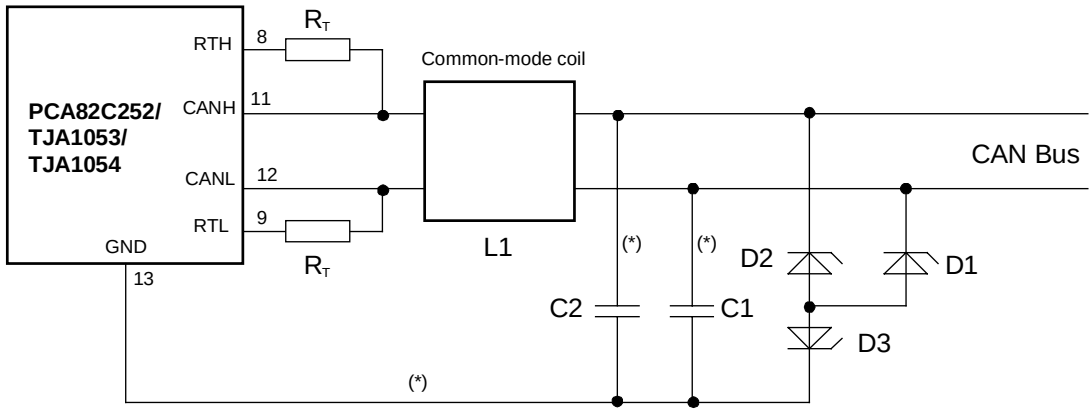
TJA1053 : P_{peak} = (27 V) ^{2} / 1000 Ohms = **730 mW** for less than **60 us** (Ex 13.2)

TJA1054 : P_{peak} = (27 V) ^{2} / 1000 Ohms = **730 mW** for less than **8 ms** (Ex 13.3)

Because this peak current does flow for a very short time only, it typically has no relevance for dimensioning the termination resistors. Most important is the average power dissipation for the TJA1054 (23,7 mW) and the maximum continuous power dissipation for the TJA1053 / PCA82C252 (64 mW) since these are the worst case conditions for the corresponding devices.

5. ESD Protection Circuit Concept

The purpose of the presented circuit approach is to limit the peak voltages being present at the IC pins CANH and CANL of the fault-tolerant CAN transceiver when a CAN bus line is being subjected to ESD pulses.



L1 = up to 70 uH, e.g. ACT3225 or ACT4532 (TDK) or B82790-S0513-N201 (Siemens) or equiv.
D1 = D2 = D3 : stand-off voltage > max. bus line DC voltage, e.g. BZG04-27 or equiv. for bus line voltages ≤ +27V
C1 = C2 = 100 pF to 330 pF
(*) Note: minimize inductance & length of C1 and C2 leads